Hardware simulator of Caliste-SO detectors for STIX instrument

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ABSTRACT

The Spectrometer Telescope for Imaging X-rays (STIX) is one of 10 instruments on-board Solar Orbiter mission of the European Space Agency (ESA) scheduled to be launched in 2017. STIX is aimed to provide imaging spectroscopy of solar thermal and non-thermal hard X-ray emissions from 4 keV to 150 keV using a Fourier-imaging technique. The instrument employs a set of tungsten grids in front of 32 pixelized CdTe detectors. These detectors are source of data collected and analyzed in real time by Instrument Data Processing Unit (IDPU). In order to support development and implementation of on-board algorithms a dedicated detector hardware simulator is designed and manufactured as a part of Electrical Ground Support Equipment (EGSE) for STIX instrument. Complementary to the hardware simulator is data analysis software which is used to generate input data and to analyze output data. The simulator will allow sending strictly defined data from all detectors' pixels at the input of the IDPU for further analysis of instrument response. Particular emphasis is given here to the simulator hardware design.

Keywords: X-ray spectrometer, simulation, detector, front-end ASIC, FPGA

1. INTRODUCTION

In 2011 ESA made a decision to perform the mission to the Sun that will give a chance for new discoveries. The selected mission is the Solar Orbiter which is equipped with 10 scientific instruments among which there is an instrument that will provide observations of solar flares in Hard X-ray (HXR) range, namely The Spectrometer Telescope for Imaging X-rays (STIX) [1]. Mission is scheduled to be launched in 2017, and after three years of cruise phase it will reach a nominal, highly elliptical orbit with aphelion distance of 0.9 AU, and perihelion distance less than 0.3 AU. The hard X-ray observations conducted by STIX will determine the intensity, spectrum, timing, and location of solar hard X-ray sources. Simultaneous measurements of all of these parameters will contribute to understanding the electron acceleration mechanism in the solar corona and their transport through the interplanetary space. In this way, STIX will provide an important link between the remote and in-situ instruments of the Solar Orbiter mission.

The STIX instrument consists of three mechanically separate parts: an X-ray transparent window in the heat shield, an imager containing 32 subcollimators and a spectrometer with 32 cadmium telluride (CdTe) Caliste-SO X-ray detectors [2], one behind each subcollimator. The STIX X-ray windows are a prime element in the instrument thermal control system, reflecting and radiating out the most of incident radiation. Its other role is to absorb too intense flux of low energy X-rays (in comparison with harder X-ray flux) that would otherwise contribute to pulse pile-up in the case of large solar flares. To obtain the hard X-ray images STIX uses collimator based Fourier imaging. Specially designed

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subcollimator grids will allow reconstructing the source image with very good angular resolution of 7 arcsecond which will give unprecedented 1000 km of spatial resolution at perihelion. The imager is also equipped with aspect system which is used to measure the offset between the STIX Instrument Line of Sight and the spacecraft's aspect system. The last part of the instrument is a Detector/Electronics Module (DEM) containing mechanical attenuator, CdTe detectors with front-end electronics [3], Instrument Data Processing Unit (IDPU) [4] and Power Supply Unit (PSU).

Solar flares, the main target of STIX observations, arise as a result of an abrupt conversion of magnetic into different forms of energy (e.g. thermal, kinetic etc.) which are observed in the solar atmosphere in every wavelength range, from radio up to gamma rays [5]. The energy released during solar flare may be as high as 10^{26} J. Such huge amount of energy may be released during dozen minutes only. It means that the X-ray flux measured at the distance of 1 AU may exceed 10^{-3} W m^{-2}. Solar flares are observed in solar atmosphere (photosphere, chromosphere and low corona), but there are several accompanying phenomena that may be present also in the interplanetary space, like Coronal Mass Ejections (CME) and Solar Energetic Particles (SEP).

Therefore Solar Orbiter mission is very challenging. Close proximity to the Sun can be hazardous for the instruments. The instrument design should take into consideration an intense solar thermal flux as well as strong X-ray flux, and energetic particles coming from the solar flares also can threaten the spacecraft. STIX will be operational in such environment and will play an important role in early detection of flares for entire spacecraft. Since the Solar Orbiter during its orbiting around the Sun will not be constantly seen from the Earth, the IDPU has to work fully autonomously. Therefore special care must be taken during development of the flight software which needs to handle all typical scenarios as well as exceptional cases. The on board algorithms will provide a number of important functions. As the on-board algorithms are critical for the instrument operation, they need to be tested carefully before launch. To fully understand the measurements made by STIX and better prepare the ground and on-board software the hardware simulator of the Caliste-SO detectors is being developed. Such detector simulator will give the unique possibility to inject the strictly defined data at the input of IDPU in order to perform functional tests. The event sequence to be applied at the input of IDPU can be prepared as so called artificial sequence (e.g. ramp signal) to perform specific tests of the individual IDPU subsystems as well as the scientific sequences that simulate real conditions such as quiet Sun or flares. Besides the test and verification purposes the simulator will also be suitable for analysis of the overall instrument response and performance.

The hardware detector simulator will be one of the instrument specific components of the Electrical Ground Support Equipment (EGSE) for STIX. The simulator is an important part of broader complex instrument simulations. This work is carried out within the framework of another STIX-related activity that covers the scientific simulation of entire data flow beginning from solar originate population of photons passing through the instrument model and resulting in telemetry data seen as the IDPU output. These simulations combine software simulation modules of imaginary sources as well as the hardware components such as detector simulator and IDPU. The simulation will allow us to better understand the instrument response taking into account various effects that contribute to measured data including instrumental effects such as pile-up, dead time or even secondary radiation from mechanical components of the instrument calculated using GEometry ANd Tracking (GEANT4) toolkit [6] developed at CERN. From the scientific point of view the pre-launch instrument simulations and analysis are the key for understanding the data obtained during the mission and their further interpretation.

2. COMPLEX INSTRUMENT SIMULATION

The block diagram of the complex instrument simulations is shown in Figure 1. It can be divided into several important steps:

1. simulations of solar X-ray emission sources,
2. simulations of optical channel,
3. simulations of photon interaction in semiconductor detectors,
4. simulations of front-end electronics response,
5. injecting the data to IDPU using hardware detector simulator,
6. data handling with real IDPU,
7. comparison of output data with input photon population.

2. 1 Simulations of solar X-ray emission sources

Imaging observations of solar flare HXR emission showed that usually few individual are observed simultaneously. Typically, all patches are concentrated in the small region with diameter that rarely may exceed area of 2 arcmin^2. However, there are situations when solar flares occur almost simultaneously in different parts of the solar disk. The field of view of the STIX instrument is equal to 4º, therefore the instrument will "see" X-ray flux coming from widely separated sources connected to different flares. Even photons from one flaring event can originate from different locations: the loop-top and foot points which can be very well distinguished with 7 arcseconds angular resolution of STIX. Taking all above into consideration the physical sources simulator will allow simulating many sources of different shapes and sizes present simultaneously across solar disc.

This step will be performed using the scientific analysis software for STIX that is developed by several international institutions as a part of Solar SoftWare library (SSW). To simulate the sources we will use real observations of solar flares obtained by Ramaty High Energy Solar Spectroscopic Imager (RHESSI) ([7], [8]). The simulation scheme is as follow.

First, we define the number of sources that we want to model on the visible solar disc. In this step we assume that the source is monochromatic, and its intensity is determined for single time interval of given length. Each source is parameterized with its monochromatic intensity, FWHM size, and shape (point, elliptic, loop-like). At present version of simulations we do not apply any temporal changes of shape, and position of the source.

Second, we intend to include the spectral information for every source and/or every patch. For this purpose we will use RHESSI spectra obtained for real solar flares. We fit to observed count spectrum with functions which will constitute the analytical form of solar flare spectrum which is described with few parameters only. Having the analytical form of spectrum will be very important, since we can easily obtain spectra with desired energy resolution, namely 0.1 keV or better.

The third step is to assign time to each photon that falls on the STIX entrance window. Having spectral fits to RHESSI data for an entire flare we have a set of parameters which characterize the spectra for consecutive time intervals. Time evolution for each parameter may be interpolated to the desired time resolution, 0.1 s or higher. These parameters describe the solar flare spectrum variability, so we can calculate the number of photons in given energy and time bin. Afterwards the photon arrival times are generated as random with Poisson distribution. As a result the photon population is created based on the current spectral distribution for given time period.

The generated population is a series of photons as seen in front of the instrument entrance window. Each photon is specified by its arrival time, energy and direction of incidence. The whole population is randomized on the STIX entrance window which gives additional two numbers defining each photon: x and y position in the entrance window. Thus, we have a seed population that will be used in the next step.

2.2 Simulations of an optical channel

A STIX optical channel consists of two main parts. First is a thermal baffle that attenuates low energy photons below 4 keV. The second is an optical tube with grids mounted at the front and similar set of grids slightly tilted at the back. This system will select Fourier components of actual emission distribution which can be used for an image reconstruction. As a geometry of the instrument is well known we can use ray-tracing and calculate if the photon of energy E, falling on the entrance window at position [x,y] will pass through front and rear grids and reach one of the detectors at a given position. Alternatively, we will use the GEANT4 toolkit to perform calculations of photon path in more complicated way which will take into account, for example, scattering of photons in the optical tube.

Both mentioned methods give the same result - the position at which photon hits the sensor. The position referenced to the local coordinate system of each individual sensor is converted to the pixel number. Once the detector and pixel at which the interaction took place is determined the direction of photon incidence is no longer applicable for the next stages of the simulation.

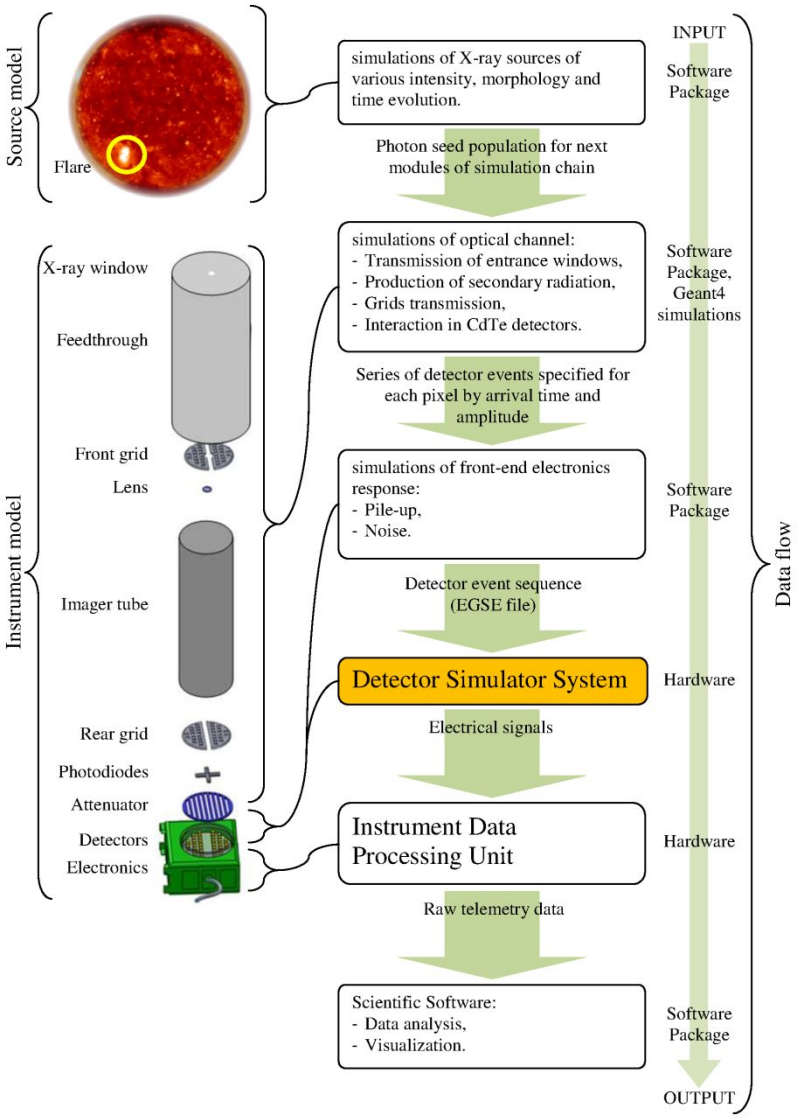

Figure 1. Block diagram of the complex instrument simulations

2.3 Simulations of photon interaction in the semiconductor detectors

Photons which passed through the beryllium windows and grids can hit CdTe sensors resulting in an interaction within the semiconductor or they can pass through without any interaction. The probability of photon absorption depends on the photon energy and corresponds to the detector efficiency. In order to take into account the efficiency some portion of photons is rejected randomly according to the given distribution and they are no longer processed. In such scenario the efficiency is calculated on the basis of a model where photo-electric effect dominate, and the detector is assumed to be infinite planar. This method will allow including attenuation by the detector entrance windows (Pt layer), effects connected with single Compton scattering (scattered photon will escape), and escaping by fluorescent photons.

As calculations mentioned above will not allow calculating edge effects we will perform GEANT4 simulations of the interaction of HXR photons in the CdTe detectors. The edge effects cannot be calculated directly in GEANT4 toolkit

however, the exact coordinates of the photon absorption in the semiconductor detector may be obtained. Thus, having the coordinates of the absorption the edge effects can be calculated using dedicated software.

2.4 Simulations of front-end electronics response

The simulated photons absorbed in the CdTe detectors induce electric signals at sensors electrodes. These signals are processed by detector front-end electronics to shape pulses with the amplitudes corresponding to the photons energies. The front-end electronics introduces two effects that need to be taken into account: pulse pile-up in case of intense flares and electronics noise. Since these effects are not simulated by the simulator hardware, they need to be calculated using dedicated software module based on the characteristics of STIX front-end electronics and their fixed parameters. It is done based on data from previous simulation stage before passing it to the hardware detector simulator.

2.5 Injecting the data to IDPU using hardware detector simulator

The detector simulator is a hardware device which allows injecting to IDPU an arbitrary detector event sequence taken as the output of STIX detector module. The simulator will be equipped with representative interfaces, so that the simulator can be directly connected to the IDPU as an equivalent of real detector module. Complete detector simulator system consists of simulator hardware and workstation equipped with dedicated software. More detailed description of the detector simulator is included in chapter 3.

2.6 Data handling with real IDPU

The IDPU includes Field Programmable Gate Array (FPGA), data and software storage memories, operating memory, housekeeping system and several interfaces to detector module, attenuator, aspect system, PSU and spacecraft. The central element of the IDPU is a FPGA from Actel's RTAX S/SL family, with loaded on a Leon 3FT processor and several state machines required by above mentioned subsystems. The FPGA is connected to an Electrically Erasable Programmable Read Only Memory (EEPROM) for storing Start-Up software, a Random Access Memory (RAM) used as a rotating buffer for data coming from the detectors and as an operation memory for the application software. There is also 16 GB Flash memory serving as an archive memory for scientific data. The IDPU controls the detectors and collects data from them. These data are processed by on-board data handling algorithms. Some of these algorithms are supported by low level state machines in FPGA, while some are handled by high level software application running on the processor. The on-board algorithms perform data selection and compression based on the solar flare detection and adaptive algorithms, supplemented by specific requests from the ground. Other data processing functions include: quick-look of a data accumulations; live-time measurements; background monitoring; on-board coarse flare location; acquisition of aspect system data; and the quiet-time long-term accumulation of background counts to monitor the detector energy calibration. The output from the IDPU in a form of a selected quick-look data or special requested data set is forwarded to the Payload Data Management Unit.

2.7 Comparison of output data with input photon population

The IDPU is accessed using a Spacecraft Instrument Interface Simulator (SIIS) or SpaceWire (SpW) interface in order to command the IDPU and collect the output data. The scientific and housekeeping data are monitored using dedicated EGSE software or they are converted to FITS files that can be used as an input for science analysis software. The analysis of output data using the EGSE software allows verifying whether the data have been correctly processed by the IDPU. Using the science software the spectra, light curves and reconstructed images may be compared directly with the simulated sources. As every module of the data flow is controlled we are able to analyze the influence of particular factors end effects on the output data stream.

3. SIMULATOR DESIGN

3.1 Caliste-SO detection unit of STIX instrument

The detection unit of STIX, called Caliste-SO integrates functions of X-ray absorption with a CdTe semiconductor sensor and analog front-end electronics with a full custom ASIC named IDeF-X HD [9]. The sensor of 10x10 mm^2 area and 1 mm thickness is subdivided into 8 large and 4 small pixels arranged into four stripes required for the detection of the Moire pattern projected by grids system. These 12 pixels are surrounded by guard ring. The IDeF-X HD ASICs includes 32 analogue channels consisting of Charge Sensitive Amplifier (CSA) with a continuous reset system, a variable gain stage (Gain), a Pole-Zero cancellation stage (PZ filter), a variable shaping time second order low pass filter (RC^2 Filter), a Baseline Holder (BLH), a peak detector (Peak Det), and a discriminator. Each of 12 pixels and guard ring are bounded to one of analogue channels. The remaining 19 channels of the ASIC are unused and are powered off. The ASICs are also equipped with special digital serial link for chip configuration and readout. The serial interface allows connecting up to 8 ASICs in parallel using shared signals of a single chip. The ASIC link uses four signals to interface with the controller. These are: DIN, STROBE, DOUT and TRIG. All of them are LVDS type. All communication between IDeF-X HD and its controller is synchronized with the STROBE signal driven by the controller. In general there are three main types of communication between IDeF-X HD and its controller: global sequence, slow control and readout. The global sequence is used to initiate communication and to specify the next action to be performed: slow control or readout. The slow control allows configuring ASICs parameters such as gain or shaping time by writing to the internal chip registers. The readout is performed in order to forward the analogue value of pulse amplitude from peak detector to the analogue output AOUT. Since the AOUT is common for all ASIC channels, the amplitudes from individual channels are multiplexed. When the pulse amplitude is present at the AOUT, it can be digitized by external A/D converter connected to the ASIC.

These 32 Caliste-SO units in the STIX are organized in four quarters. Each quarter contains 8 units. Additionally each group of two Caliste-SO are connected in parallel in order to reduce number of connection between detector module and IDPU. Each group is connected to one common A/D converter, thus there are four ADCs per quarter. Each detector quarter is also equipped with a pair of main and redundant auxiliary temperature sensors.

The IDPU provides all interfaces to communicate with all Caliste-SO groups and their ADCs. The role of IDPU is to perform three key tasks. Firstly, the IDPU configures all Caliste-SO units after power on by the slow control communications. This is necessary since the IDeF-X HD ASICs use default configuration settings after power on and those settings differ from the optimal ones selected for STIX operation. Secondly, during normal instrument operation, the IDPU continuously performs read-outs from all Caliste-SO units. Each time when X-ray photon detected by Caliste-SO has energy greater than discriminator level the TRIG signal is asserted to notify the IDPU that there is an event to be read-out. The IDPU detects these triggers from all Caliste-SO groups and sends a series of control signals to ASICs and associated A/D converters. These cause the conversion of the analog voltage levels that are proportional to X-ray energy to 12-bit digital values. The third IDPU task is to collect housekeeping data. In case of detector module these are temperatures of the individual detectors read from IDeF-X HD ASICs (only in non-flare mode) and detector PCB temperature measured by mentioned auxiliary temperature sensors.

3.2 Architecture of detector simulator

The architecture of STIX spectrometer determines the detector simulator design. The simulator must be seen by the IDPU as real STIX detector module including IDeF-X HD ASICs and A/D converters selected for STIX instrument. Therefore the simulator architecture has similar structure. There are also four quarters containing 8 ASICs models and 4 ADCs models. Similarly, they are connected in parallel in groups of two ASICs models and one associated A/D converter model as well. All signals that are specific for ASICs and ADCs are the same as in their real counterparts. The auxiliary temperature sensors are also simulated. All these simulator features allow the IDPU to perform the same actions as with the real detector module.

The architecture of detector simulator hardware is shown in Figure 2. The simulator consists of three main parts: simulator controller, memory storage and detector quarters. The controller part includes USB 2.0 interface and simulator engine implemented in main FPGA indicated as FPGA #1 in the Figure 2. The controller performs several key functions.

These are communication with workstation via USB connection, managing the memory storage and distributing simulation data to the detector quarters during the simulation process. The USB interface consists of specialized chip and dedicated state machine (SM) indicated as USB SM in the Figure 2. The USB state machine is running at 60 MHz clock provided by USB interface chip while the rest of FPGA logic is running at main system clock of 50 MHz. For that reason all data transferred between workstation and the simulator are buffered using FIFO queues that separate two different clock domains in main FPGA. The other role of the FIFOs is to ensure proper data flow when reading or writing to memory storage as the data are transferred in 512 bytes blocks. The USB connection is used to control the simulator and to upload the simulation data to the memory storage with data rate up to 30 MB/s.

Each quarter has its own interface to the IDPU which contain ASICs and ADCs signals, temperature sensors signals, Single Event Upset (SEU) signal, test pulse signals and power related signals. The power signals are also routed to main FPGA to detect if the quarter is powered. If no, the respective quarter can be disabled.

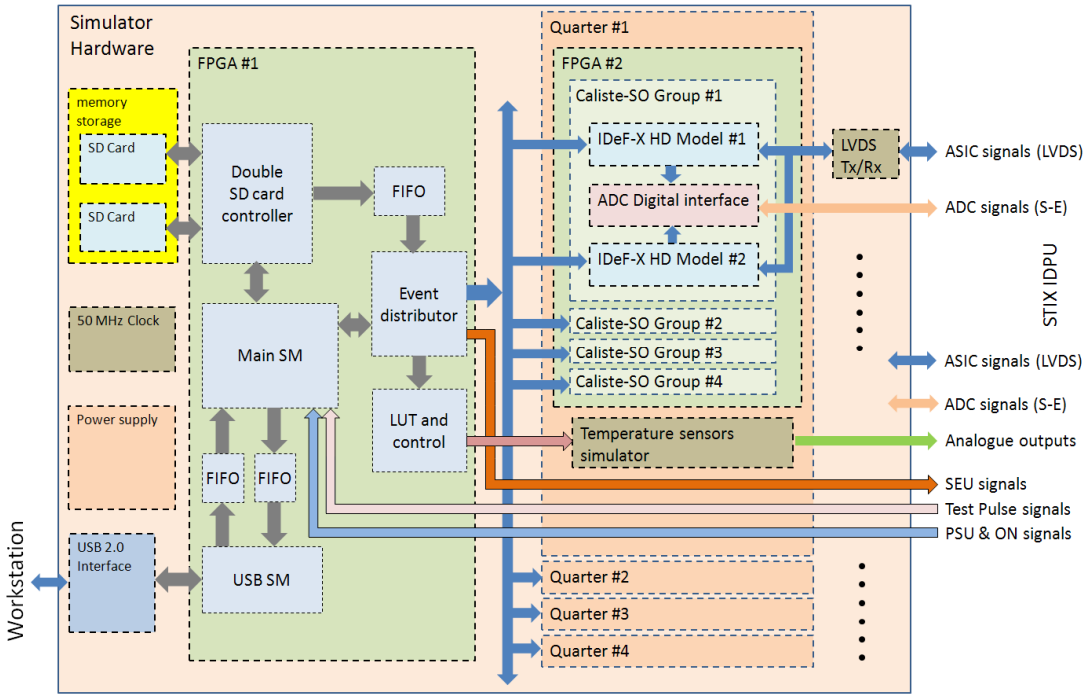

Figure 2. Block diagram showing the architecture of detector simulator hardware.

The main state machine indicated as main SM in the Figure 2 handles the data sent from workstation. The simple communication protocol and data formatting allows the main SM to distinguish commands from other data. The main state machine interprets and executes the commands such as starting and stopping the simulation or data reading and writing to memory storage.

The detector quarters use separate FPGAs to contain ASICs and ADCs models, thus there are five FPGAs in the simulator: the main FPGA as the controller and four FPGAs in detector quarters. All FPGAs selected for the simulator design are Xilinx XC3S1400A chips in FTG256 packages. For the simulator development a dedicated breadboard shown in Figure 3 has been manufactured. The breadboard has the same structure as shown in Figure 2, but includes only one detector quarter. Additionally it uses smaller Xilinx XC3S400 FPGAs. The breadboard is used for development of all FPGA IP cores, the workstation software and for verification of individual subsystems hardware. It can be also used as the simulator prototype with limited number of simulated detectors.

The final design will be divided into separate modules such as: power supply, controller board and four pieces of detector quarter. These modules will be manufactured in Euro card standard format, so that they can be mounted in modular 3U enclosure and connected using dedicated backplane.

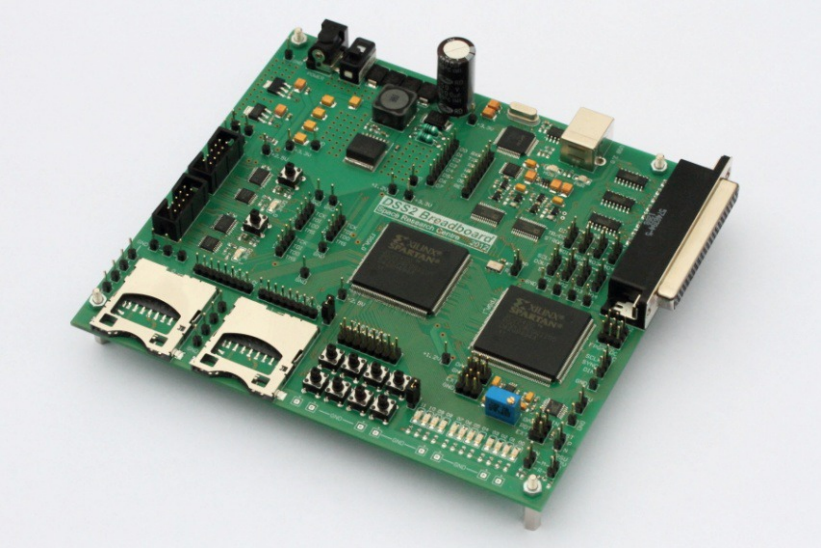

Figure 3. Breadboard of detector simulator.

3.3 ASICs and ADCs models

Both ASICs and ADCs models were developed as IP cores to be implemented in FPGA. They were written in VHDL base on IDeF-X HD ASIC and A/D converter documentation respectively. Unlike the real ASIC, the model has only digital part covering communication interface and control state machine, ASICs internal registers and additional logics that allows injecting data to the model. The models do not simulate analogue part of the real IDeF-X HD ASICs. The analogue signal that represents output of peak detector in real ASIC is replaced in model with 12-bit digital value that correspond to respective analogue signal digitized by A/D converter. The model has an additional amplitude register to store the digital value of peak detector as seen by IDPU after A/D conversion. This approach has two advantages: model simplification and possibility to provide to IDPU strictly defined digital data without any losses of precision caused by additional A/D conversion. On the other hand, as there is no pulse shaping, the model does not simulate such effects as electronic noise and pile-up by itself. However, these effects can be modeled prior and added to simulated event sequence before passing it to IDPU.

The ASIC model contains all 13 internal registers that are implemented in real ASIC. All of these registers have the same widths, addresses, names and default values as in real ASIC. They can be written and read by slow control operations in the same manner as in real ASIC. Some of them take part in the simulation and may affect the simulator output while some are meaningless. For example the ALIMON register is used to control powering the channels. Obviously, the channels that are not powered cannot produce any output. The register is also examined in the model and the events are passed only through these channels which are powered according to the ALIMON value. Other register that may affect the simulator output is TH register that sets the thresholds of amplitude discriminators. Implemented is also 32-bit event register storing the information which channels have been triggered. The register plays the same role as in real ASIC.

A single group of two ASIC models in parallel with common ADC model is implemented in FPGA as shown in Figure 4. All signals on the right side are standard ASIC and ADC signals that connect real STIX detector module with IDPU. The differential signaling for ASIC model is provided by external LVDS physical-layer transceivers. All signals on the left side except NUMASIC are simulator specific signals used for injecting data by simulator engine to the ASIC models. The NUMASIC is a standard ASIC input used to assign ASIC address when operating in parallel. The asynchronous RESET input clears all amplitude registers, event register, set default values in ASIC configuration registers and reset the model to initial state. 12-bit AMPLITUDE input is used to write a value to one of 32 amplitude registers that correspond to peak detectors in real ASIC. Each channel has an individual amplitude register. A short pulse on HIT input writes the value from AMPLITUDE input to the amplitude register in the channel specified by 5-bit NUMCHANNEL input. The AMPLITUDE and NUMCHANNEL inputs are common for all ASIC models within the

simulator while the HIT inputs are individual for each ASIC model. It means that the event can be written only to one channel within one ASIC model at ones. The amplitudes are written only if the following conditions are met:

- ASIC model is in detection phase,
- the channel of target pixel is powered (ALIMON register is examined),
- amplitude discriminator of target pixel is not disabled (TH ≠ 63),
- event amplitude is greater than threshold set in TH register,
- event amplitude is greater than the amplitude already written.

Once the amplitude is written to the amplitude register, the TRIG out and respective bit in event register are set to logical '1' and afterwards the event can be read by the IDPU. All communication with the model can be performed at STROBE frequency of 20 MHz which is nominal for real IDeF-X HD ASIC.

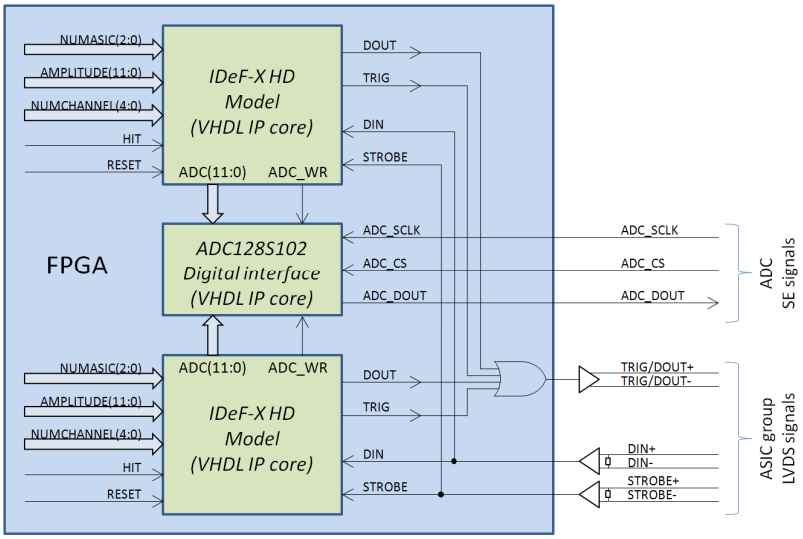

Figure 4. Block diagram of two ASIC models in parallel with single ADC model implemented in the simulator FPGA.

The ADC model includes a 12-bit register with parallel inputs and serial output. When the IDPU initiates readout action and the ASIC model enters the readout phase, the values stored in amplitude registers are loaded successively to the ADC model. These values can be read subsequently by the IDPU using ADC representative serial interface. This operation corresponds to multiplexing the analogue peak amplitudes to analogue output in real ASIC during the readout phase in order to digitize them using real ADC.

3.4 Memory storage

The simulator is equipped with a non-volatile memory storage for storing the event sequences. These sequences contain big amount of detector events, thus the size of single sequence can be of order of several GB. In addition, during the simulation the data need to be read continuously with relatively high peak bit rates. For that reason the memory storage within the simulator serves as the memory buffer that ensures required data rate. As the sequence data are big in size it takes some time to upload them to the simulator therefore the memory storage is non-volatile, so that the data are kept even after power off and on cycle.

The memory storage is based on two SDHC cards. The cards are driven simultaneously to ensure higher data rate than in case of a single card. It requires using a pair of the same type of cards. Maximum supported capacity of a single card is up to 32 GB, thus total space available for sequences amounts to approximately 60 GB. Such capacity allows storing sequence of about 8×10^9 events which corresponds to sequence duration from ~7 to ~180 hours of instrument operation in orbit depending on average event rate.

The SDHC cards controller was developed as IP core implemented in main FPGA. The cards operate in UHS-I High Speed mode using 4-bit data bus at clock frequency of 50 MHz. This gives real data rate of approximately 44 MB/s which is fast enough for simulator operation with reasonable margin. The controller does not support any file system on the cards, but operates using low level direct access to 512 bytes data blocks. For that reason the event sequence cannot be saved on SD cards directly from workstation, but only by uploading the sequence from the workstation to the simulator. The low level access is necessary to obtain required data rate by performing sequential reading and writing.

3.5 Detector event sequence

The data to be injected to IDPU coming from previous stages of simulation are arranged as a series of detector events called detector event sequence. Each event in the sequence is specified by discrete arrival time referenced to the start time of the simulation. The nominal time step of the simulation Δt, amounts to 20 ns and this is the shortest time interval between successive events. During the simulation the successive events appear at the simulator output on given times specified by the event arrival times. All events in the sequence must be sorted by arrival time in ascending order. In addition the arrival times must be unique. It is not allowed to assign the same arrival times to two or more events. The simulator hardware does not support multiple events on one discrete time. Only one event can be released on one discrete time. However the multiple events are simulated as a group of several events separated in time by single time step Δt. From the simulation point of view such approach is acceptable. After receiving TRIG signal the IDPU waits for latency time before starting the readout. All events that arrive within the latency time are seen by IDPU as one multiple event. The latency time is long enough to inject the amount of simulated events that is sufficient for simulation purposes.

The event sequence can contain six types of events foreseen for the simulator operation:

1. Detector event - specified by arrival time, detector number, pixel number and amplitude.
   The event causes triggering of single pixel within single detector model as it was done by an X-ray photon hitting the real Caliste-SO sensor.

2. ASIC temperature sensor event - specified by arrival time, detector number, and the temperature.
   The event sets the temperature value as seen by internal temperature sensor within ASIC. The temperature can be read by IDPU as housekeeping data.

3. Test Pulse event - specified by arrival time and pulse amplitude.
   The event sets the amplitude that will be read by IDPU when applying test pulse at the ASIC input for test charge injection. This feature of ASIC is used in STIX instrument and IDPU can perform such test.

4. Auxiliary temperature sensor event - specified by arrival time, sensor number and the temperature.
   The event sets the temperature values as seen by auxiliary temperature sensors mounted in STIX detector module. The temperatures can be read by IDPU as housekeeping data.

5. SEU event - specified by arrival time and detector number.
   The event activates SEU signal that simulates SEU output of real Caliste-SO unit. The signal informs the IDPU that SEU occurred in some of Caliste-SO units within given quarter.

6. Dummy event - specified by arrival time.
   The event does nothing. Using this event is required for some timing issues arising from simulator architecture.

The events are encoded on 32-bit value regardless of their type. All event types have fixed data order and they are distinguishable by the simulator. The detector events fill the most of event sequence as they carry the scientific data. Their arrival times are critical for simulations because of many timing issues that may affect the data as seen by IDPU. The ASIC temperature sensor event and auxiliary temperature sensor event carry the housekeeping data. As the IDPU reads the temperatures regularly, they need to be refreshed with at least the same rate. However the arrival times of the temperature related events are not critical. The Test Pulse and SEU events will be used very sporadically only for special tests.

3.6 Principle of operation

The simulator controller includes so called event distributor implemented in FPGA. During the simulation the distributor reads successively the event sequence from memory storage and distributes individual events over all detector models. The successive detector events are released by the distributor on precise event arrival time. In case of auxiliary temperature sensor events, they are distributed to the respective subsystem that simulates the temperature sensor. The event distributor includes a time counter and a comparator. During the simulation, the time counter is running continuously at the 50 MHz clock. The arrival time of the first awaiting event in the queue is compared to the time counter. When both times are equal, the event is released and the next event is fetched from the queue. The distributor extracts from processed event the information on event type and its parameters. Based on this information, the event is distributed to appropriate detector model or simulator of temperature sensor.

The principle of simulator operation is shown in Figure 5. In this example four detector events are released on given arrival times. This causes asserting of TRIG signals by respective detector models. These signals notify the IDPU about the event to be read and remain until the event readout is initiated. For clarity the figure shows only four detector groups within one detector quarter. In reality there are sixteen detector groups in the simulator and the sequence can contain billions of events.

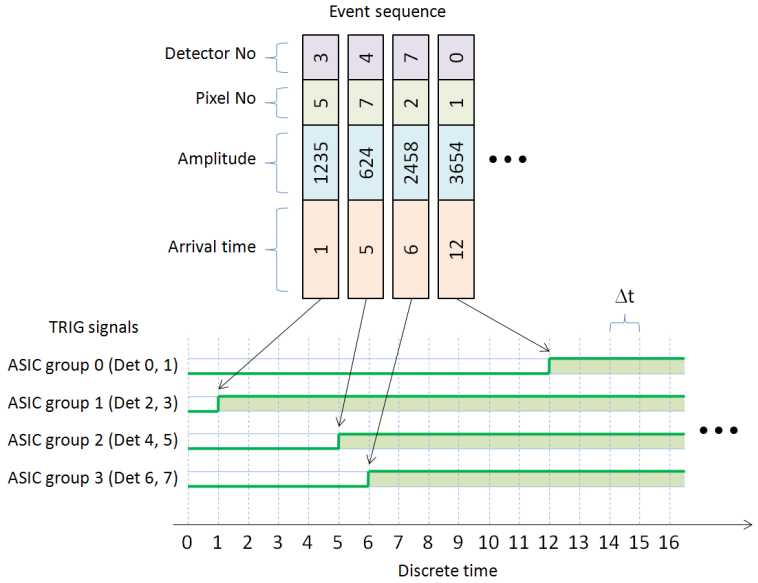

Figure 5. Principle of simulator operation.

STIX instrument has its own autonomous mechanisms that prevent the observed count rate to be greater than 20 000 c/s for each detector in order to avoid pile-up during strong flares. The limiting of measured count rate is done by covering the detectors using mechanical attenuator and/or disabling pixels. The expected detectors count rates determines a requirement for the detector simulator that should be capable to generate detector events with rate of at least 20 000 events per second for each detector or even more. It requires the hardware to be able to generate detector events with total rate greater than 640 000 events per second for all 32 detectors. Such event rate corresponds to data rate of about 2.5 MB/s. The event data can be read from memory storage with much greater data rate of about 44 MB/s, thus the requirement is met with a large margin. In addition the events transferred from the memory storage to the event distributor are buffered using fast FIFO queue to mitigate possible irregularity of the memory storage reading. The event queuing also increases the peak event rate that can be achieved for short time periods in order to handle multiple events.

3.7 Simulator of temperature sensor

The detector simulator includes eight simulators of auxiliary temperature sensors mounted in STIX detector module. These are thermistor sensors seen by IDPU housekeeping as variable resistance. The sensors exhibit strongly nonlinear

resistance in function of a temperature. Therefore in order to cover entire range of the resistance with sufficient accuracy a single simulator uses three digital potentiometers of 1 MΩ, 100 kΩ and 10 kΩ in parallel. Each of them operates in rheostat mode. The resistance of individual rheostat is set by 8-bit data resulting in 256 possible settings. Additional SHDN signal is used to set the potentiometer in open circuit state. The resultant resistance of parallel rheostats is determined by set of three 8-bit values and SHDN signals. These settings have been determined only for selected temperatures covering entire sensor range with 1°C step and included as a look-up table in main FPGA. On auxiliary temperature sensor event, the temperature is converted to respective rheostat settings and subsequently the rheostats are configured using I^2C interface.

3.8 Simulator software

The simulator software runs on a workstation connected to the simulator hardware using USB connection. It is designed only as a user interface to control the system by sending commands to the simulator hardware and simple visualization of simulator state. Neither workstation nor software will take part directly in the event generation process. They will be used only to manage the event sequence data, to upload the sequences from workstation to the simulator hardware and to start/stop the generation process which will be performed purely by simulator hardware in real time.

4. SUMMARY

STIX is a hard X-ray spectrometer and imager. The Fourier imaging technique is used in the instrument and is here significantly improved by using pixelized Caliste-SO detection units. The instrument will provide the observations of solar flares in HXR range that allows understanding the electron acceleration mechanism in the solar corona and their transport through the interplanetary space. To support the instrument development a complex instrument simulations are being prepared. The simulation will cover entire data flow beginning from solar photon population at origin passing through the instrument model and resulting in data seen at the instrument output. The novelty simulation approach combines a software simulation of sources based on RHESSI data, a simulation of STIX imager and sensors using GEANT4 toolkit and finally injecting the simulated data to STIX IDPU using dedicated hardware detector simulator. In this way, obtained output data can be compared with known input sources characteristics in order to carry out the analysis of instrument response. For that purpose a dedicated hardware simulator of Caliste-SO detectors is being developed as the component of the STIX EGSE.

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